IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. NXP SEMICONDUCTORS N.V., et al.. Defendants.	Case No. 7:24-cv-00028-DC-DTG

PLAINTIFF'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. Introduction

U.S. Patent No. 8,549,339 (the "'339 Patent") teaches an innovative multi-core processor with sets of processor cores. In particular, the '339 Patent teaches various means of coordinating not just the individual cores of the multi-core processor but the sets of processor cores that operate as a unit. While previous techniques focused on coordination among individual cores, the '339 Patent focuses on coordination as to sets of cores.

Defendant's arguments ignore this focus. Despite agreeing that "set of processor cores" means a "group of two or more processor cores," Defendant fails to apply this definition properly. Instead, Defendant reads a disavowal of any single-reference-oscillator architecture, where the Applicant explains how the prior art does not teach *sets* of processor cores. Both references only teach sending a single, unprocessed clock signal to anything that could be considered a "set" of processors. The Applicant explained as much. Thus, Defendant's purported "word-for-word" construction is drawn from disparate descriptions of the prior art to create a limitation the applicant never intended.

Defendant's indefiniteness arguments fare no better. First, a POSITA would readily understand the meaning of "configure[] to dynamically receive." Second, the term "periphery" has sufficient meaning and is not a term of degree. Third, the phrase "a common region that is substantially central" is well-disclosed by the specification.

II. Disputed Terms Requiring Construction

a. Term 1: "the first clock signal is independent from the second clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Plain and ordinary, meaning, where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks**

The claim term "the first clock signal is independent from the second clock signal" is straightforward and does not require additional construction beyond its plain and ordinary meaning. Defendant, however, proposes an unnecessary and restrictive construction which contradicts both the plain meaning of the term and the prosecution history. Defendant's "word-for-word" construction is nowhere to be found in the prosecution history. Instead, the applicant made it clear that the use of "independent" is best understood as simply meaning "different." Defendant draws its flawed construction from a misunderstanding of both the claim language and the prior art.

During prosecution, the applicant amended the claims to clarify the relationship between the clock signals and the PLLs, specifying that the first and second clock signals are inputs to separate PLLs associated with different sets of processor cores. The examiner initially rejected claims reciting "a first set of processor cores … configured to dynamically receive … a first clock signal; a second set of processor cores … configured to dynamically receive … a second clock

signal," in view of Jacobowitz and Kim[1]. Dkt. No. 39-7. In response, the applicant made several amendments including to add the disputed term. Notably, however, the first and second clock signals of the original claim are not the same signals as in the disputed term. Rather, the original first and second clock signals became the first and second *output* clock signals of the first and second PLLs while the new first and second clock signals of the disputed term are the *inputs* to the PLLs. Dkt. 39-9 at 3.

Original Claim Language	Amended Language
1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each dynamically receive a first supply voltage and a first clock signal; A second set of processor cores of the multi-core processor, wherein each processor core form the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input; A second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

[1] Jacobowitz refers to U.S. Publication No. 2009/0106576 (Dkt. No. 39-5). Kim refers to U.S. Publication No. 2009/0138737 (Dkt. No. 39-6).

Put in terms of Figure 3 from the specification, the clock signal of the original claim referred to the arrow entering Core 152 while the clock signal of the disputed term refers to Clock Signal 1, 2, and/or 3. *See* Dkt. No. 39-8 ("However, the broadest reasonable interpretation of the recited claim language (i.e., claim 1: first set of processor cores configured to dynamically receive a first clock signal) reads on the clock output of the local oscillators of Jacobowitz and also reads on the output of the PLLs shown in applicant's figure 3.") In terms of Jacobowitz[2], the original clock signal was V_0 or V_1 while the clock signals of the disputed terms refer to V_R:

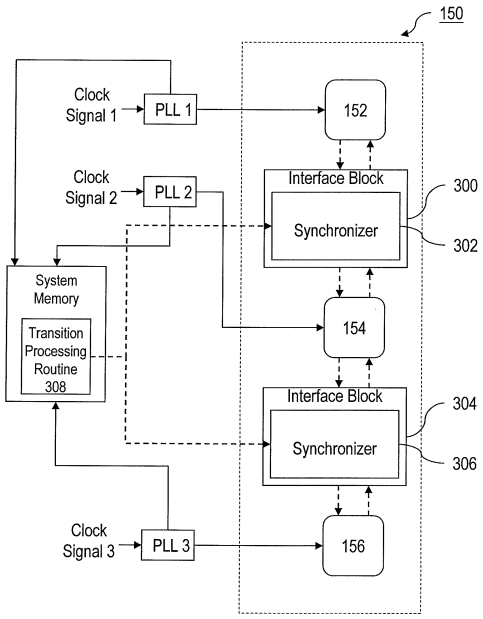

FIG. 3

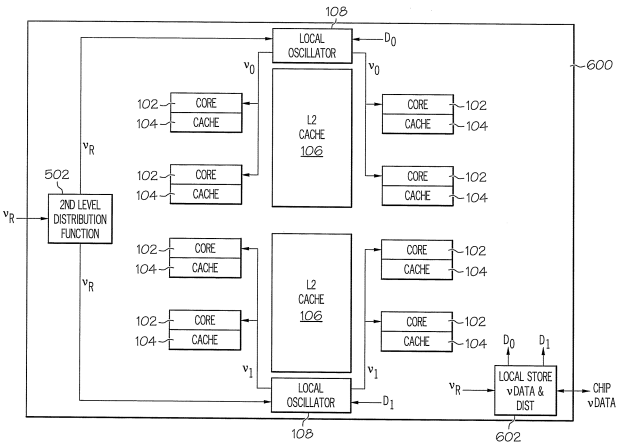

FIG. 6

'339 Patent at Figure 3; Jacobowitz at Figure 3. Because there was no distinction in the claim between the input and output signals of the PLLs, at least under the broadest reasonable interpretation, the examiner rejected any distinction that Clock Signal 1, 2, 3 were "different/independent" while V_R was only a single signal. Dkt. No. 39-8.

[2] Jacobowitz, of course, does not teach the claims and thus mapping the claimed terms to Jacobowitz is of only limited illustrative value.

Nowhere during prosecution did Applicant ever clearly disavow a single clock system, as Defendant contends. Applicant's remarks were focused on the clock signal as an *input*. Dkt. No. 39-9 at. 9-10 ("Jacobowitz clearly show[s] that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (V_R) and distributes V_R to local oscillators 108. [] Jacobowitz fails to disclose or teach … a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input, respectively." (emphasis in original)). As to Kim, the applicant did not even argue independence of the signals was distinguishing, merely acknowledging it as a limitation. *See Id*. at 10 ("In addition , Kim also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal.")

What the Applicant did describe was the absence of any "set of processor cores" in either Jacobowitz or Kim. That is the first and most important distinction over both pieces of prior art—not a single clock system. The Applicant explained that, while Jacobowitz mentions that "[f]urther power management can be realized by controlling supply voltage (Vdd) to each core and/or chip," this statement does not provide any reference to "sets of processor cores"—only to individual cores. *Id*. at 9. Likewise for Kim, the applicant explained: "Kim discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4})." *Id*. at 10. This *was* clear disavowal, and Plaintiff and Defendant accordingly have agreed to a construction of "set of processor cores."

Despite Defendant failing to demonstrate any clear disavowal as to "independent," it nonetheless still contends that construing the disputed term is necessary to avoid permitting the claims to cover the "exact arrangement" of Jacobowitz and Kim. Dkt. No. 39 at 10. However, neither reference teaches the "arrangement" supposedly motivating Defendant's proposed construction. In particular, there is no basis to insert the phrase "or processed (i.e. divided or multiplied) from a single reference oscillator clock." No prior art considered in the prosecution teaches providing such a first and second clock signals to a respective first and second PLLs associated with a first and second set of processor cores. First, Jacobowitz does not discuss processing the signal of the reference clock before reaching the first and second PLLs. Instead Jacobowitz provides the unprocessed signal directly to the Local Oscillators. *See* Jacobowitz at ¶¶ [0037] - [0038]. In contrast, while Kim does teach processing a single reference oscillator clock with a main PLL having multiple frequency dividers prior to reaching further PLLs, only the main PLL is taught to be associated with multiple cores. Kim at ¶ [0024]. Kim does not teach providing processed signals from a single clock source to multiple sets of processor cores as claimed. Defendant's construction does not prevent "recapture" of any considered prior art.

Defendant's further discussion of "multiple and independent" is also unavailing. Even if "independent" is not coextensive with "multiple," it does not follow that "independent" must mean "provided by or processed (i.e., divided or multiplied) from [different] reference oscillator clocks." This logical leap has no basis in the prosecution history. Defendant ignores that the only occasion the Applicant used the phrase "multiple and independent" was in reference to the "resuming communications" limitation of claims 15 and 18 not claim 1. Dkt. No. 39-9 at 11. In any case the Applicant also reemphasized that neither Jacobowitz nor Kim teach "sets of processor cores." Dkt. No. 39-9 at 11. The Applicant explained neither reference "discloses having *sets* of processor cores

configured to receive multiple and independent clock signals." *Id*. (emphasis added). As Kim does not have sets of processor cores at all and is the only source for the "processed (i.e., divided or multiplied)" language, finding a clear disavowal here is improper.

If the Court finds that "independent" needs clarification—it does not—it merely means "different." This is the term that the applicant used interchangeably with "independent" and is what the examiner clearly understood it to mean. *See* Dkt. No. 39-8 ("Applicant's representative referred to figure 3 of the specification and stated that clock signals 1 through 3 were different/independent clock signals input to the PLLs…"(emphasis added)). Defendant's attempt to redefine "independent" is inconsistent with both the applicant's amendments and examiner's understanding.

b. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Indefinite**[3]

Defendant argues because "configured to dynamically receive" does not have a common understanding in the field and "dynamically" is "vague," the disputed term is indefinite. This argument is unfounded.

First, the phrase "configured to dynamically receive" is plainly understandable to a POSITA. Both the advantages and difficulties of dynamically providing voltage and clock signals

[3] Plaintiff notes that while Defendant MediaTek and Defendant NXP argue the next three terms are indefinite and make similar arguments, the arguments are not identical and are supported by different experts.

to processor cores in a multi-core processor were well known in the art by the time of the priority date. For example, the patent explains that "dynamically adjusting the power profile for a stripe in response to changes in computational requirements may reduce power consumption for a multi-core processor." '339 Patent at 3:16-20. Further, the face of the patent cites at least one paper detailing how to manage this dynamic change. *See* Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages[4] ("Cheng[5]"). If a POSITA would understand dynamically *providing* voltage and clocks, they would also understand dynamically *receiving*, which is merely the complementary action.

While the exact phrase "configured to dynamically receive" is not found in the specification, that is not required. *See e.g. ESCO Grp. LLC v. Deere & Co.*, No. CV 20-1679-WCB, 2023 WL 4199413, at *14 (D. Del. June 22, 2023) (Bryson, C.J.). "[C]onfigured to dynamically receive" is not some term of art with a specialized meaning separate and apart from its component terms. It merely refers to the set of processor cores being configured to receive changing voltage and clock signals, such as for jobs with differing computational demands.

Even Dr. Villasenor recognizes that "configured to dynamically receive" relates to the power consumption management of a multi-core processor. Dkt. No. 39-1 at ¶ 66. Dr. Villasenor's criticism that the specification is "silent on *how* the sets of processor cores may themselves be 'configured to dynamically receive,'" conflates *enablement* with claim construction. *Id*. (emphasis added). This issue at hand is not whether the patent describes *how* to achieve the configuration but whether a POSITA would understand the meaning of the term. Moreover, even a cursory review of the patent provides at least one example of how such configurations could be achieved. Dynamic

[4] This paper was cited on the face of the patent and therefore is intrinsic evidence. *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005).
[5] Cheng is included herewith as Ex. 1 to Mirzaie Declaration.

Voltage and Frequency Scaling circuits with Two Supply Voltages "presents circuits that enable dynamic voltage and frequency scaling (DVFS) for fine-grained chip multi-processors to reduce both dynamic and leakage power dissipation." Cheng at 1236. Cheng details one such configuration that would enable a processor core to receive changing power profiles that was known in the art:

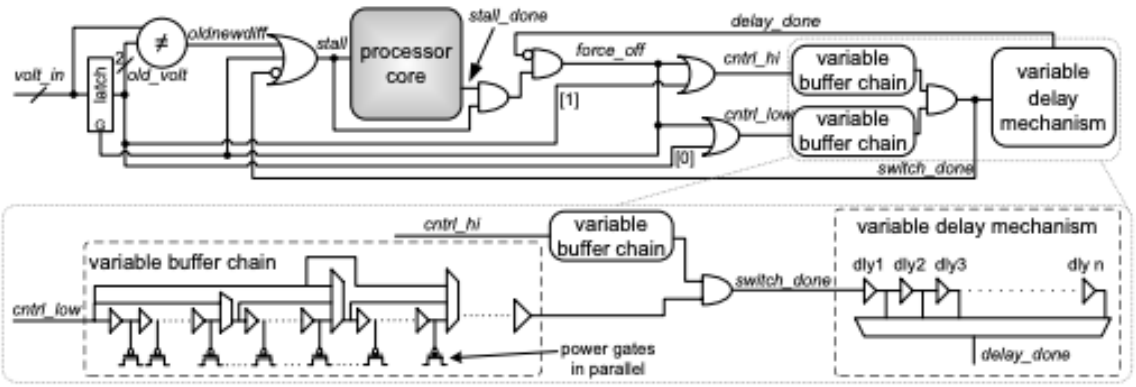

Fig. 4. Configurable dynamic run-time voltage supply switching circuit for the DVFS controller shown in Fig. 2

Id. at 1238. This is one configuration that might allow a set of processor cores to dynamically receive a first supply voltage and a first output clock signal.

Defendant's argument that "dynamically" is vague is no more availing. Defendant has *no* support for even the base assertion, not even their own expert. From the above, it should be clear why, "dynamically" is a frequently used term in the art referring to changes in signals. *See e.g.* Jacobowitz at 43; Kim at 3-4; Cheng *generally*. The patent explains the kind of change in the power profile that qualifies for "dynamically" relates to the intentional changes, rather than mere fluctuations, that are used to respond to changes in computational requirements. *See* '339 Patent at 3:16-56. A POSITA would be readily familiar with the term.

Defendant's comparison to claim 5 is irrelevant. Claim 5's reference to "configured to receive one or more control signals" relates a specific connection to "control blocks located in a

periphery" not the overall configuration of a set of processor cores as in the independent claim. The cited language serves a different function than the disputed term. The language of claim 5 does not reference a changing signal as "dynamically" does. They are simply not comparable.

Defendant has failed to show that "dynamically," a frequently used term in the art, is so vague that a person skilled in that art could not reasonably ascertain the meaning of "configured to dynamically receive." The patent sufficiently explains the context and purpose of the term. It is clear that it relates to the necessary configurations to receive changing power profiles.

c. Term 3: "located in a periphery of the multi-core processor"

'339 Patent Claims	**Redstone's Proposed Construction**	**Defendant's Proposed Construction**
Claims 5	**Plain and ordinary meaning**	**Indefinite**

Defendant next argues that because it cannot determine a singular construction of a "multi-core processor" and because "periphery" is a term of degree without guidance, the disputed term is indefinite. These arguments fail on both fronts.

The patent clearly describes a "multi-core processor." The first line of the patent provides an example of a "multi-core processor," which "includes two or more independent processor cores arranged in an array." '339 Patent at 1:6-7. Claim 1 describes a particular multi-core processor with a first and second set of processor cores and an interface block coupled to both sets. *See id*. at Cl. 1. The patent goes further to illustrate the multi-core processor in Figure 1. *Id*. at 1:26-27.

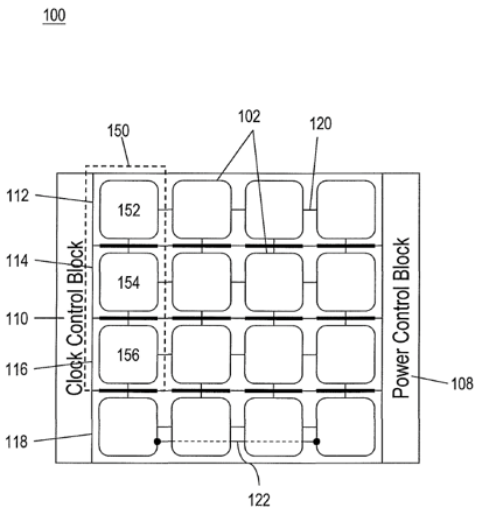

FIG. 1

In Figure 1, the various cores are depicted as 102 with a potential set 150 of cores 152, 154, and 156 where all cores are interconnected through an interface circuit 120. *See id*. at 2:4-40; 3:16-26. Dr. Villasenor suggests that Figure 1, by depicting a "multi-core processor" containing the control blocks, further confuses what a "multi-core processor" is. Dkt. No. 39-1 at ¶ 80. Not so. The description of the figure provides guidance. The specification provides that "[i]n some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multi-core processor 100 as shown in FIG. 1." '339 at 2:34-36. The specification thus clarifies the metes and bounds of the multi-core processor, placing the control blocks at its edge.

Dr. Villasenor's further attempts to confuse this clear disclosure should be disregarded. First, Dr. Villasenor ignores the clear disclosure discussed above to opine that a POSITA might also consider the packaged die or packaged chip as the multi-core processor. *See* Dkt. No. 39-1 at ¶¶ 75-77. This contention is supported by no analysis of the specification, the claims, or any discussions in the industry, just Dr. Villasenor's bald opinion. *Id*. Considering, the question is "[i]f

the claims when read *in light of the specification* reasonably apprise those skilled in the art of the scope of the invention," *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed. Cir. 2001) (emphasis added), an opinion that ignores the specification should be disregarded. Unsupported conjecture about what a POSITA would understand cannot meet the Defendant's burden to overcome the presumption of validity.

Second, Dr. Villasenor imagines a distributed architecture whose periphery he contends cannot be ascertained. He contends that "[i]f one view the collection of processor cores alone as the 'multi-core processor' of the claims, with stripes of Figure 1 arranged in the manner depicted in Figure C, a POSITA would not understand with reasonable certainty what constitutes the periphery of such a multi-core processor." Dkt. No. 39-1 at ¶ 82. But Dr. Villansenor offers no analysis to support his conclusion and never addresses the claim language. According to claim 1, the multi-core processor comprises a first set of processor cores, a second set of processor cores, and an interface block coupled to both sets not "the collection of processor cores alone." '339 Patent at Cl. 1. Dr. Villasenor's Figure C does not depict at least the interface block. Without depicting all parts of the claimed multi-core processor of course one cannot ascertain a periphery. If one were to imagine there is an interface block coupled to what Dr. Villasenor has labeled the third and fourth sets of processor cores physically located between them, it become readily apparent that the periphery would be along the rectangle one could draw around all three components, as illustrated below:

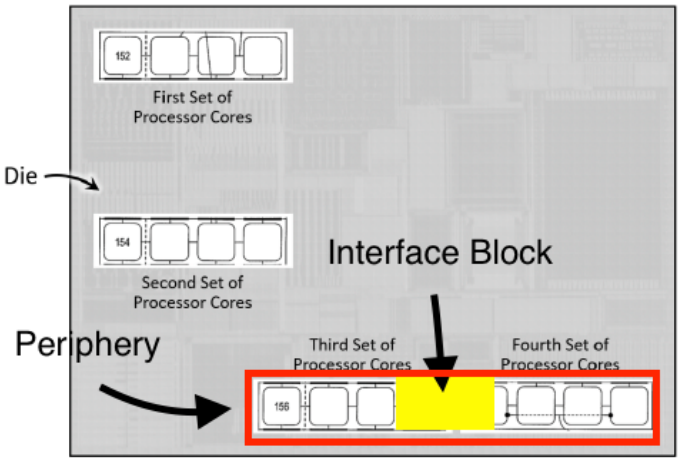

Figure C

While one might imagine much more unique and bizarre architectures, again, the test asks if in light of the specifications, is "periphery of the multi-core processor" reasonably clear to one of skill in the art. It is.

Defendant's further attorney argument that "periphery" is a term of degree is likewise unavailing. It is not. It is a relational term. In this case it defines an area in relation to the multi-core processor. By way of analogy, no one would suggest that "outdoors" is a term of degree because it is supposedly unclear whether a person in the process of walking through the door is "outdoors" or not. "Outdoors" is neither a term of degree nor vague, the hypothetical merely raises an edge case where the factual determination is difficult. The same is true of "periphery."

A POSITA readily understand the scope of "located in a periphery of the multi-core processor." As noted above, "periphery" is a well-known relational term used in relation to a well-defined term "multi-core processor." The disputed term should be given its plain and ordinary meaning.

d. Term 4: "located in a common region that is substantially central to the first set of cores and second set of processor cores"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 14	Plain and ordinary meaning	Indefinite

Here, Defendant's twofold arguments that both "located in a common region" and "substantially central" are individually indefinite, both fail. Defendant contends "substantially central" is a term of degree without sufficient notice of scope while "common region" simply has no ascertainable meaning from the specification. Neither are true.

First, "located in a common region" is clear to a POSITA. Rather than merely relating to an undefined area, "region" is used throughout the patent to refer to sections of the multi-core processor. *See* '339 Patent at 2:20-21 ("The multi-core processor 100 may be further divided into regions.") The specification explains these regions may "correspond to rows of the two-dimensional array, and the regions may or may not be overlapping." *Id*. at 2:22-23. These "two-dimensional array[s]" are the rows of processors or stripes that can make up sets of processor cores. *Id*. at 2:24-27. This use is continued throughout the claims. *See e.g. id*. at Cl. 8 ("wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.") A POSITA would understand that a "region" corresponds with the subdivision of the multi-core processor containing the claimed sets of processor cores.

Understanding that the claimed "region" contains the control blocks and is a subdivision of the multi-core processor relating to sets of core processors, the meaning of "common region" becomes clear. "Common region," rather than being a term of art, merely references a region

common to the first and second sets of processor cores. *See id*. at Cl. 14. While different architectures will dictate different forms for such a region, a POSITA would understand the scope of "common region."

Even Defendant recognizes "common region" refers to a part of the multi-core processor shared by the first and second sets of processor cores, though Defendant attempts to discredit it through claim differentiation. Dkt. No. 39 at 14-15. However, claim differentiation as a doctrine cannot be used to support a finding of indefiniteness. Claim differentiation creates a *rebuttable* presumption of non-redundant claims. *See Comark Communications, Inc. v. Harris Corp*., 156 F.3d 1182, 1187, 48 U.S.P.Q.2d 1001 (Fed. Cir. 1998) ("While we recognize that the doctrine of claim differentiation is not a hard and fast rule of construction, it does create a presumption that each claim in a patent has a different scope."). The Federal Circuit has explained that this cannon is not an absolute, "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically." *Power Mosfet Technologies, L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409–10, 72 U.S.P.Q.2d 1129 (Fed. Cir. 2004). Here, if, as Defendant argues, claim 14 has an overlapping meaning with claim 9, that meaning is mandated by the plain meaning and the patent itself and thus the claims should be construed identically, not indefinitely. Even if claim differentiation could result in indefiniteness, claim differentiation is inapplicable. There are a variety of other differences between claim 14 and claim 9. For instance, claim 9 does not recite "one or more control blocks" or mandate where such a block is located. Claim 14 does. Further, claim 9 recites two regions, claim 14 recites only one. With so many differences between claim 9 and 14, there is no risk that the Court finding claim 14 definite would render any claim superfluous. Considering even Defendant recognizes the scope of "common region," "common region" cannot be the basis for finding claim 14 indefinite.

Defendant's alternative basis for indefiniteness fares no better. For a "substantially" term to be definite, "[a]ll that is required is some standard for measuring the term of degree." *Exmark Mfg. Co. Inc. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018). The patent provides that guidance.

First, the claim language itself provides guidance. The claimed control blocks are located in a "common region" that is substantially central to the first and second set of processor cores. A POSITA's understanding of what a "region" is, as explained above, guides where the contained control blocks can be located. Because a "region" is a subdivision of the multi-core processor, a POSITA would understand that this is within the multi-core processor.

Second, the patent describes a number of embodiments with regard to the placement of control blocks. The patent describes three possibilities "two different sides of the multicore processor," "the same side of the multi-core processor," or "in a common area located near the center of the multi-core processor." '339 Patent at 2:31-40. Put differently, the patent describes putting the control blocks on the sides of the processor or within the processor. A POSITA would understand by contrast and example "substantially central" refers to not along the outside of the multi-core processor but the inside. When combined with a POSITA's understanding of "common region," a POSITA has a standard by which to measure "substantially central."

While Defendant attempts to muddy the water with its Figures D and E, these arguments are faulty. Most notably, neither Figure D or E shows a region beyond the disarticulated stripe regions of Figure 1. While the claimed invention can be distributed similarly to how Defendant's figures show, the figures fail to show the interconnections between the stripes such as the claimed "interface block" or the described interface circuit, *see* '339 at 2:9-19. This causes two related problems. First and most simply, there is no ability to determine if either there is a common region

or if the control blocks are within that region. Second, by showing only the sets of processor cores and the control blocks, a POSITA cannot ascertain the bounds of the multi-core processor. As claimed, the multi-core processor comprises the sets of processor cores and the interface block coupled to both. Because, as explained above, "substantially central" is measured by comparison to the bounds of the multi-core processor, without showing the multi-core processor Figures D and E are not helpful.

For these reasons, Defendant has not shown by clear and convincing evidence that Claim 14 is indefinite. Claim 14 should be given its plain and ordinary meaning.

III. Conclusion

For the reasons provided above, all disputed terms should be given their plain and ordinary meaning. Defendant has failed to meet its burden to show any term is indefinite.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that on January 8, 2025, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Reza Mirzaie
Reza Mirzaie